PIC18(L)F27/47K40

28/40/44-Pin, Low-Power, High-Performance Microcontrollers with XLP Technology

Description

These PIC18(L)F27/47K40 microcontrollers feature analog, core independent peripherals and communication peripherals, combined with eXtreme Low-Power (XLP) technology for a wide range of general purpose and low-power applications. These 28/40/44 -pin devices are equipped with a 10-bit ADC with Computation (ADCC) automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and performing automatic threshold comparisons. They also offer a set of core independent peripherals such as Complementary Waveform Generator (CWG), Windowed Watchdog Timer (WWDT), Cyclic Redundancy Check (CRC)/Memory Scan, Zero-Cross Detect (ZCD) and Peripheral Pin Select (PPS) providing for increased design flexibility and lower system cost.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input over the full V_{DD} range
  - 62.5 ns minimum instruction cycle
- Programmable 2-Level Interrupt Priority
- 31-Level Deep Hardware Stack
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Four 16-Bit Timers (TMR0/1/3/5)
- Low-Current Power-on Reset (POR)
- Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

Memory

- 128K Bytes Program Flash Memory
- 3728 Bytes Data SRAM Memory

- 1024 Bytes Data EEPROM
- Programmable Code Protection
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Ranges:
  - 1.8V to 3.6V (PIC18LF27/47K40)
  - 2.3V to 5.5V (PIC18F27/47K40)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operation Modes

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Extreme Low-Power mode (XLP)
  - Sleep: 500 nA typical @ 1.8V
  - Sleep and Watchdog Timer: 900 nA typical @ 1.8V

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Windowed Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals

- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:
  - Two CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- 10-Bit Pulse-Width Modulators (PWM):

  - Two 10-bit PWMs
- Serial Communications:
  - Two Enhanced USART (EUSART) with Auto-Baud Detect, Auto-wake-up on Start. RS-232, RS-485, LIN compatible
  - SPI
  - I^2C, SMBus and PMBus™ compatible
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change on all pins
  - Input level selection control
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash or EEPROM
  - High-speed or background operation
- Hardware Limit Timer (TMR2/4/6+HLT):
  - Hardware monitoring and Fault detection
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)

Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADC^2):
  - 35 external channels
  - Conversion available during sleep
  - Four internal analog channels
  - Internal and external trigger options
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - 8-bit hardware acquisition timer
- Hardware Capacitive Voltage Divider (CVD) Support:
  - 8-bit precharge timer
  - Adjustable sample and hold capacitor array
  - Guard ring digital output drive
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Programmable 5-bit voltage (% of V_{DD},[V_{Ref+} - V_{Ref-}], FVR)
  - Internal connections to comparators and ADC
- Two Comparators (CMP):
  - Four external inputs
  - External output via PPS

- Fixed Voltage Reference (FVR) Module:
  - 1.024V, 2.048V and 4.096V output levels
  - Two buffered outputs: One for DAC/CMP and one for ADC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if external clock stops
- Oscillator Start-up Timer (OST)

Programming/Debug Features

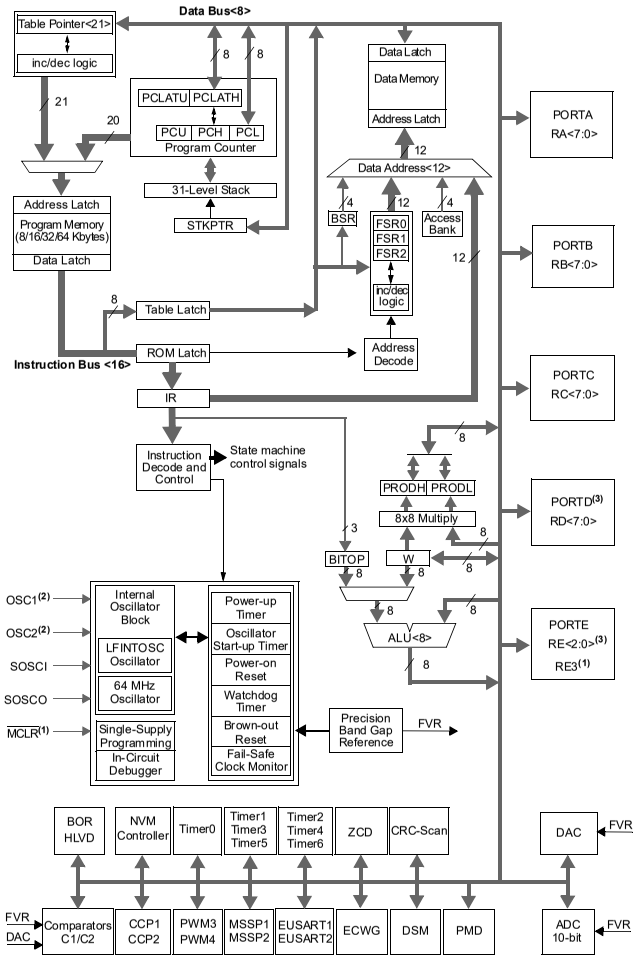
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

PIC18(L)F27/47K40 Family Types

Table 1. Devices included in this data sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	I/O Pins	16-bit Timers	Comparators	10-bit ADC^2 with Computation (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	SMT	Low Voltage Detect (LVD)	8-bit TMR with HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I^2C/SPI	PPS	Peripheral Module Disable	Temperature Indicator	Debug(1)
PIC18(L)F27K40	128k	3615	1024	25	4	2	24	1	1	2/2	1	0	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18(L)F47K40	128k	3615	1024	36	4	2	35	1	1	2/2	1	0	1	3	Y	Y	2	2	Y	Y	Y	I

Figure 1-1. PIC18(L)F27/47K40 Family Block Diagram



Note 1: RE3 is only available when $\overline{MCLR}$ functionality is disabled.
2: OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes.
3: PORTD and PORTE<2:0> not implemented on 28-pin devices.

Figure 10-1. Program and Data Memory Map

Address	Device				
	PIC18(L)Fx4K40	PIC18(L)F25/45K40	PIC18(L)F65K40	PIC18(L)Fx6K40	PIC18(L)Fx7K40
Note 1	Stack (31 Levels)				
00 0000h	Reset Vecor				
...	...				
00 0008h	Interrupt Vecor High				
...	...				
00 0018h	Interrupt Vecor Low				
...	...				
00 001Ah to 00 3FFFh	Program Flash Memory (8 KW)	Program Flash Memory (16 KW)	Program Flash Memory (16 KW)	Program Flash Memory (32 KW)	Program Flash Memory (64 KW)
00 4000h to 00 7FFFh	Not Present(2)				
00 8000h to 00 FFFFh		Not Present(2)	Not Present(2)		
01 0000h to 01 FFFFh				Not Present(2)	
02 0000h to 1F FFFFh					Not Present(2)
20 0000h to 20 000Fh	User IDs (8 Words)(3)				
20 0010h to 2F FFFFh	Reserved				
30 0000h to 30 000Bh	Configuration Words (6 Words)(3)				
30 000Ch to 30 FFFFh	Reserved				
31 0000h to 31 00FFh	Data EEPROM (256 Bytes)	Data EEPROM (1024 Bytes)			
31 0100h to 31 01FFh	Unimplemented				
30 000Ch to 30 FFFFh	Reserved				
3F FFFCh to 3F FFFDh	Revision ID (1 Word)(4)				
3F FFFEh to 3F FFFFh	Device ID (1 Word)(4)				

Note 1: The stack is a separate SRAM panel, apart from all user memory panels.
2: The addresses do not roll over. The region is read as '0'.
3: Not code-protected.
4: Device/Revision IDs are hard-coded in silicon.

Figure 10-8. Data Memory Map

Bank	BSR<3:0> addr<11:8>	addr<7:0>	PIC18(L)F									
			24k40	25k40	26k40	27k40	45k40	46k40	47k40	65k40	66k40	67k40
0	0h	00h-5Fh										
		60h-FFh										
1	1h	00h-FFh										
2	2h	00h-FFh										
3	3h	00h-FFh										
4	4h	00h-FFh										
5	5h	00h-FFh										
6	6h	00h-FFh										
7	7h	00h-FFh										
8	8h	00h-FFh										
9	9h	00h-FFh										
10	Ah	00h-FFh										
11	Bh	00h-FFh										
12	Ch	00h-FFh										
13	Dh	00h-E9h										
		EAh-EEh										
		EFh-FFh										
14	Eh	00h-87h										
		88h-8Ch										
		8Dh-8Fh										
		90h-9Fh										
		A0h-FFh										
15	Fh	00h-5Fh										
		60h-FFh										

Virtual Access Bank
00h-5Fh
60h-FFh

GPR
SFR
Unimplemented