Chapter 0

Presentation

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2021-2022

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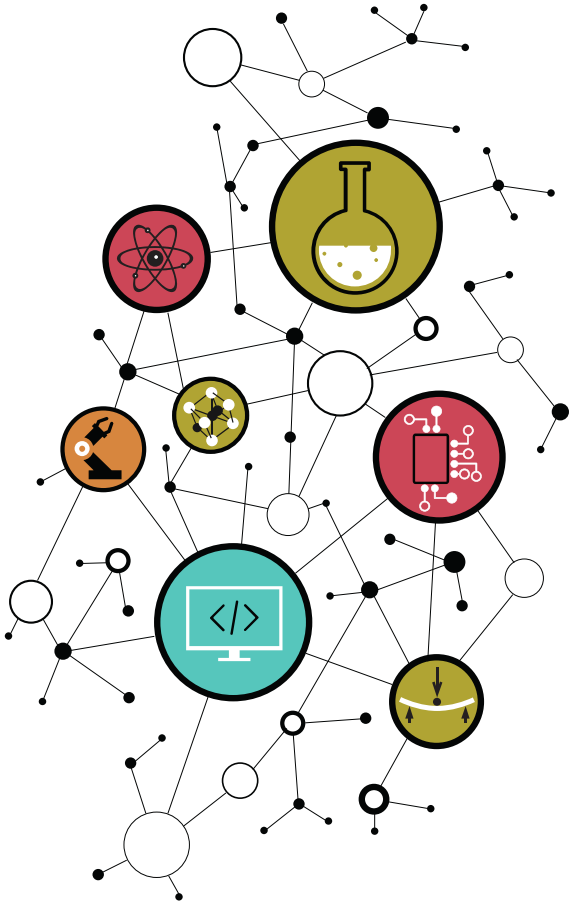

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Using our knowledge on MCUs, understand why and how Digital Signal Processors were designed and still used

→ Application to DSPs, using the Texas Instruments' C6600

Using our knowledge on GPPs, understand how to use a parallel architecture in order to improve the computing performances

→ Application to parallel programming, using OpenMP with a classical Intel Core iX GPP

Keywords: DSP, GPP, architecture, OpenMP, parallel computing.

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Part I – Session 1, Dimitri Boudier

Lectures (4 h)

Chapter 1 – Diversity of Processor Architectures

Chapter 2 – Texas Instrument C6678 Architecture

Chapter 3 – Lab algorithm

Chapter 4 – Texas Instrument C6678 Assembly language

Practical labs (21 h)

Implement the same algorithm in different ways (standard C, C6600-specific C, C6600 assembly, …) and compare their performances.

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Part II – Session 3, Emmanuel Cagniot

Lectures (1 h)

Practical labs (9 h)

Use the OpenMP over an existing C program in order to use the GPP parallel architecture and improve the program performances.

All the material can be found on Moodle in free access:

https://foad.ensicaen.fr/course/view.php?id=924

Development tools are also on Moodle:

Tools list with their version number and download link are updated on the Moodle page.

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Lab examination

1h – Optimising algorithm performances using one of the methods learned in the labs.

Be careful, understand what you do and why it is done that way.

No examination for the Part II (parallel programming on GPP, E. Cagniot).