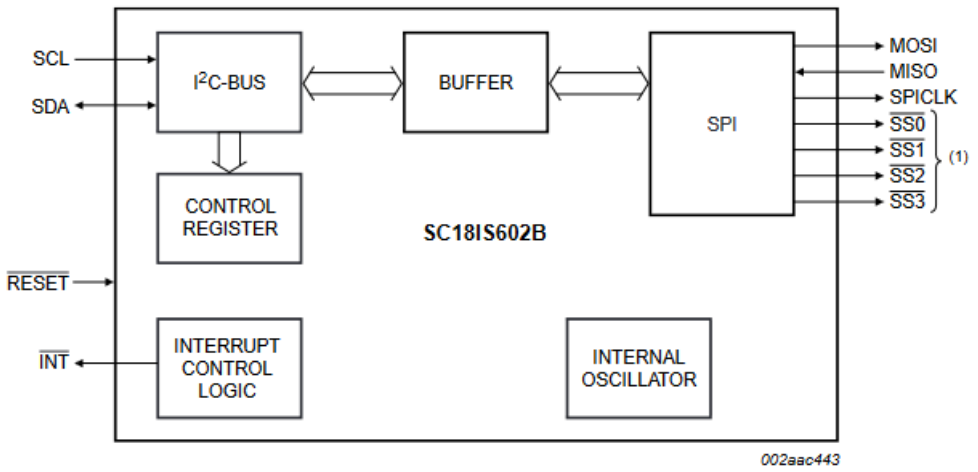
Block diagram



(1) Unused slave select outputs may be used for GPIO.

Fig 1. Block diagram of SC18IS602B

Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
$\overline{SS0}$/GPIO0	1	I/O	SPI slave select output 0 (active LOW) or GPIO 0
$\overline{SS1}$/GPIO1	2	I/O	SPI slave select output 1 (active LOW) or GPIO 1
$\overline{RESET}$	3	I	reset input (active LOW)
V_{SS}	4	-	ground supply
MISO	5	I	Master In, Slave Out
MOSI	6	O	Master Out, Slave In
SDA	7	I/O	I²C-bus data
SCL	8	I	I²C-bus clock
$\overline{INT}$	9	O	Interrupt output (active LOW). This pin is an open-drain pin.
$\overline{SS2}$/GPIO2	10	I/O	SPI slave select output 2 (active LOW) or GPIO 2
SPICLK	11	O	SPI clock
V_{DD}	12	-	supply voltage
$\overline{SS3}$/GPIO3	13	I/O	SPI slave select output 3 (active LOW) or GPIO 3
A0	14	I	address input 0
A1	15	I	address input 1
A2	16	I	address input 2

Addressing

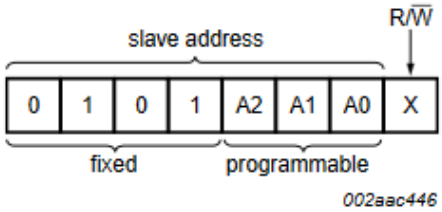


Fig 4. Slave address

The first seven bits of the first byte sent after a START condition defines the slave address of the device being accessed on the bus. The eighth bit determines the direction of the message. A ‘0’ in the least significant position of the first byte means that the master will write information to a selected slave. A ‘1’ in this position means that the master will read information from the slave. When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/W bit.

A slave address of the SC18IS602B is comprised of a fixed and a programmable part. The programmable part of the slave address enables the maximum possible number of such devices to be connected to the I2C-bus. Since the SC18IS602B has three programmable address bits (defined by the A2, A1, and A0 pins), it is possible to have eight of these devices on the same bus.

The state of the A2, A1, and A0 pins are latched at reset. Changes made after reset will not alter the address.

When SC18IS602B is busy after the address byte is transmitted, it will not acknowledge its address.

Write to data buffer

All communications to or from the SC18IS602B occur through the data buffer. The data buffer is 200 bytes deep. A message begins with the SC18IS602B address, followed by the Function ID. Depending upon the Function ID, zero to 200 data bytes can follow.

The SC18IS602B will place the data received into a buffer and continue loading the buffer until a STOP condition is received. After the STOP condition is detected, further communications will not be acknowledged until the function designated by the Function ID has been completed.

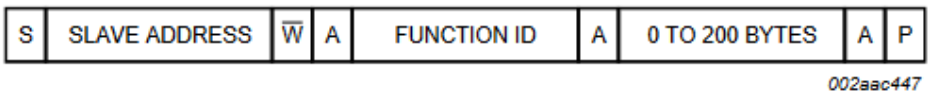


Fig 5. Write to data buffer

Read from buffer

A read from the data buffer requires no Function ID. The slave address with the R/W bit set to a ‘1’ will cause the SC18IS602B to send the buffer contents to the I2C-bus master. The buffer contents are not modified during the read process.

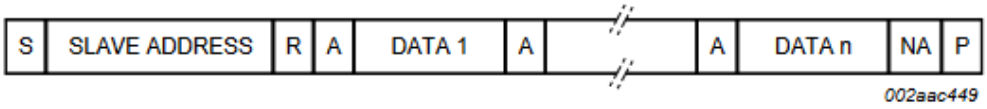


Fig 8. Read from buffer

Clear Interrupt - Function ID F1h

An interrupt is generated by the SC18IS602B after any SPI transmission has been completed. This interrupt can be cleared (INT pin HIGH) by sending a ‘Clear Interrupt’ command. It is not necessary to clear the interrupt; when polling the device, this function may be ignored.

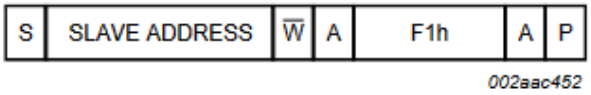


Fig 10. Clear Interrupt

Idle mode - Function ID F2h

A low-power mode may be entered by sending the ‘Idle Mode’ command.

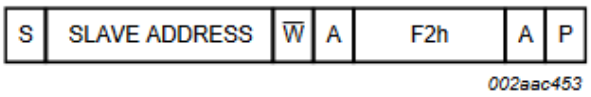


Fig 11. Idle mode

The Idle mode will be exited when its I2C-bus address is detected.

GPIO Enable - Function ID F6h

At reset, the Slave Select pins (SS0, SS1, SS2 and SS3) are configured to be used as slave select outputs. If these pins are not required for the SPI functions, they can be used as GPIO after they are enabled as GPIO. Any combination of pins may be configured to function as GPIO or Slave Selects.

After the GPIO Enable function is sent, the ports defined as GPIO will be configured as quasi-bidirectional.

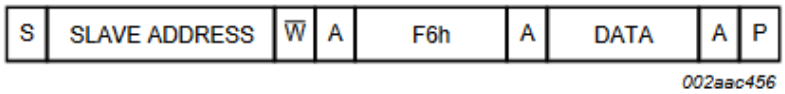


Fig 14. GPIO Enable

The data byte following the F6h command byte will determine which pins can be used as GPIO. A logic 1 will enable the pin as a GPIO, while a logic 0 will disable GPIO control.

Table 9. GPIO Enable (F6h) bit allocation

7	6	5	4	3	2	1	0
X	X	X	X	SS3	SS2	SS1	SS0

Configure SPI Interface - Function ID F0h

The SPI hardware operating mode, data direction, and frequency can be changed by sending a 'Configure SPI Interface' command to the I2C-bus.

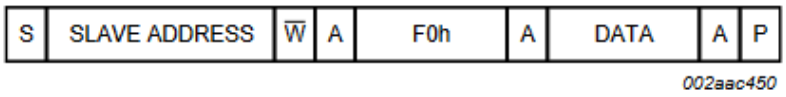


Fig 9. Configure SPI Interface

After the SC18IS602B address is transmitted on the bus, the Configure SPI Interface Function ID (F0h) is sent followed by a byte which will define the SPI communications.

The Clock Phase bit (CPHA) allows the user to set the edges for sampling and changing data. The Clock Polarity bit (CPOL) allows the user to set the clock polarity. Figure 19 and Figure 20 show the different settings of Clock Phase bit CPHA.

Table 5. Configure SPI Interface (F0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	ORDER	X	MODE1	MODE0	F1	F0
Reset	X	X	0	X	0	0	0	0

Table 6. Configure SPI Interface (F0h) bit description

Bit	Symbol	Description
7:6	-	reserved
5	ORDER	When logic 0, the MSB of the data word is transmitted first. If logic 1, the LSB of the data word is transmitted first.
4	-	reserved
3:2	MODE1:MODE0	Mode selection 00 - SPICLK LOW when idle; data clocked in on leading edge (CPOL = 0, CPHA = 0) 01 - SPICLK LOW when idle; data clocked in on trailing edge (CPOL = 0, CPHA = 1) 10 - SPICLK HIGH when idle; data clocked in on trailing edge (CPOL = 1, CPHA = 0) 11 - SPICLK HIGH when idle; data clocked in on leading edge (CPOL = 1, CPHA = 1)
1:0	F1:F0	SPI clock rate 00 - 1843 kHz 01 - 461 kHz 10 - 115 kHz 11 - 58 kHz

SPI read and write - Function ID 01h to 0Fh

Data in the buffer will be sent to the SPI port if the Function ID is 01h to 0Fh. The Function ID contains the Slave Select (SS) to be used for the transmission on the SPI port. There are four Slave Selects that can be used, with each SS being selected by one of the bits in the Function ID. There is no restriction on the number or combination of Slave Selects that can be enabled for an SPI message. If more than one SSn pin is enabled at one time, the user should be aware of possible contention on the data outputs of the SPI slave devices.

Table 4. Function ID 01h to 0Fh

7	6	5	4	3	2	1	0
0	0	0	0	SS3	SS2	SS1	SS0

The data on the SPI port will contain the same information as the I2C-bus data, but without the slave address and Function ID. For example, if the message shown in Figure 6 is transmitted on the I2C-bus, the SPI bus will send the message shown in Figure 7.

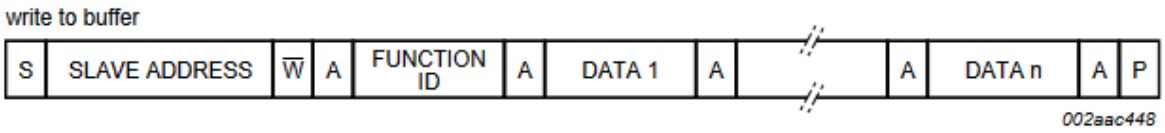


Fig 6. I²C-bus message

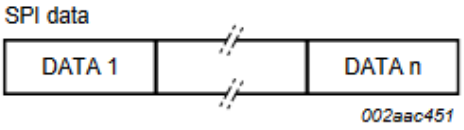


Fig 7. SPI message

The SC18IS602B counts the number of data bytes sent to the I2C-bus port and will automatically send this same number of bytes to the SPI bus. As the data is transmitted from the MOSI pin, it is also read from the MISO pin and saved in the data buffer. Therefore, the old data in the buffer is overwritten. The data in the buffer can then be read back.

If the data from the SPI bus needs to be returned to the I2C-bus master, the process must be completed by reading the data buffer.